Revolutionizing Data Path with Algorithm-Protocol Synergy

Silicon-Proven Subsystems | Host-Device Vertical Integration

STRATEGIC VALUE

- Vertical Integration: Mastery over both Host & Device interfaces with in-house ECC/PQC algorithms.
- Protocol-Algorithm Synergy: Inline hardware embedding of complex logic for zero-latency execution.
- Full-Spectrum Support: Real-time, 24/7 engineering task force for seamless SoC-level integration.

VETERAN PEDIGREE

- Frontier Node Mastery: Proven Tape-Out record from legacy 55nm to TSMC 3nm/4nm FinFET.
- Mission-Critical Quality: ISO 26262 ASIL-B aligned methodology for extreme stability.
- Elite R&D Heritage: 15+ years expertise from industry giants.

PUFiQ™: QUANTUM-SECURE HARDWARE ROOT OF TRUST (QSRoT)

PUFiQ™ is a lightweight hardware security architecture designed for closed Host-Device systems. By coupling PUF with PQC, it enables microsecond-level secure key exchange and authentication without CPU or symmetric key storage. It empowers AI and HPC systems with a protocol-level Quantum-Secure Bridge.

HIGH-SPEED INTERFACE & STORAGE IP PORTFOLIO

Category	Specification & Subsystem Integration	Foundry / Status
UFS / UniPro	UniPro 1.8/2.0 & UFS 3.1/4.0 Subsystems (Host & Device)	**TSMC 4nm / UMC 22nm Proven**
NAND Flash	NAND Controller (BCH/LDPC) & ONFI 5.2 PHY Solution	**TSMC 3/5/6nm Proven**
eMMC / SD	eMMC 5.1 & SD 6.1 Device/Host Solutions	**SMIC 40nm / 22nm Proven**
LPDDR 5/5X	High-Performance Memory Controller + Digital PHY Subsystem	**Ongoing**
Security Suite	ML-KEM, ML-DSA, AES-XTS, and PUF Silicon-IP	**Silicon Ready**

PRE-VERIFIED DATA PATH SUBSYSTEMS

- **Subsystem A: Mobile** — Integrated SD/eMMC/UniPro Device + Buffer Manager for host-side efficiency.
- **Subsystem B: NAND** — NFC + NAND PHY + Configurable ECC (BCH/LDPC) for high-reliability storage.
- **Subsystem C: Secure** — Secure High-Speed Storage (UFSHCI + UniPro + PUFiQ™ PQC Engine).
- **Subsystem D: Memory** — Customized LPDDR5/5X Controller + Digital PHY optimized for AI-driven workloads.
- **Subsystem E: CIS** — Computation in Storage: FEC + Security + Memory I/F for Near-Memory Processing.
- **Service Layer** — SoC integration consulting, MBIST/DFT, and protocol-level customization.

STRATEGIC TECHNOLOGY ROADMAP (2026-2028)

2025
SD 6.1 / eMMC 5.1
UFS 4.0 / UniPro 2.0
LPDDR 4/5/5X CTL

2026
UFS 5.0 / UniPro 3.0

2027
UCIe Chiplet (Q3-Q4)

2028
CXL Integration (Q4)

Bridging the Gap from Host to Device

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